a second means for applying a second signal to said wiring, said second signal having an opposite polarity to said first signal; and

at least one transistor provided on said substrate and connected with said gate line at a gate thereof and connected with said data line at one of source and drain thereof and connected with said pixel electrode at the other one of the source and drain [wherein said wiring is supplied with signals having an opposite polarity to those applied to said gate wiring].

E3

26. (Amended) [The] A device [of] according to claim 25 wherein [the signals] said second signal applied to said wiring have the same magnitude of voltage as [the signals] said first signal applied to said gate line.

Please add new claim 27 as follows:

E4

--27. A method according to claim 25 wherein said second signal is synchronized with said first signal.--

REMARKS

The Examiner's Official Action dated March 5, 1997 has been received and its contents carefully noted. Claims 2, 3, 21, 25 and 26 have been amended and new claim 27 has been added to more clearly define protection to which applicant is entitled. Claims 1, 5, 6 and 21-23 are independent. Accordingly, claims 1-3, 5-8, 21-22 and 24-27 are now pending in the present application and, for the reasons set forth in detail below, are believed to be in condition for allowance.

The Official Action first asserts that newly added claims 25-26 are directed to an invention that is independent from the originally claimed invention and thus withdraws these claims from consideration. In response, these claims have been amended herewith and as amended are supported by page 9, lines 20-28 (directed to Figure 1A) and page 10, lines 3-15 (directed to Figure 1B). These portions of the specification disclose that first and second signals having opposite polarities are applied to the gate line and the

wiring of the device as recited in claims 25 and 26 as amended. New claim 27 is also submitted for examination, which defines additional protection to which applicant is entitled. These claims as amended are believed to be directed to the originally presented invention and thus consideration of these claims is respectfully requested.

The Official Action next rejects claims 1-3, 21-22 and 24 as anticipated by Japanese Patent Document Number 1-156725 to Matsueda. Specifically, the Official Action refers to Figures 1 and 4 and states that the capacitance between the pixel electrode (1, 48) and the gate line (3), and the capacitance between the pixel electrode (3)[1] and the wiring (the adjacent gate line of Figure 1) are the same as each other (as apparent from Figure 1), or not more than one tenth of the sum of the area shared by the first gate line and first pixel electrode and the area shared by the second gate line and the first pixel electrode.

In response, a marked up copy of Figure 1 of Matsueda is attached. The portion highlighted in orange shows the overlap between the gate line 3 and pixel electrode 1 and the portion highlighted in blue shows the overlap between the wiring (adjacent gate line of Figure 1) and the pixel electrode 1. The overlap areas are related to the capacitance and thus the orange area is related to a capacitance C1 between the gate line 3 and the pixel electrode 1, while the blue area is related to a capacitance C2 between the adjacent gate line and the pixel electrode 1. As can be seen, the orange area is much larger than the blue area as a result of the portion of the gate line 3 extending over TFT 4. Thus, since this area is significantly larger that the blue area, the capacitance C1 will not be the same as the capacitance C2 as recited in claim 1.

Referring to claim 22, this claim recites that a difference between area shared by the first gate line and first pixel electrode (orange area) and area shared by the second gate line and the first pixel electrode (blue area) is not more than one tenth of sum of these areas. As can be seen in Figure 1, the difference in area between the orange and blue portions is that portion of gate line 3 that extends over TFT 4. This area appears

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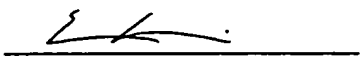
[1] Applicant notes that this should apparently be pixel electrode (1).

to be clearly more than one tenth of the sum of the orange and blue areas, and thus does not meet the limitation recited in claim 22. In any event, it is noted that Matsueda does not include any indication of the capacitance or area and thus the reference is at best unclear about whether the difference in areas is not more than one tenth of the sum of the areas as claimed.

Finally, it is noted that claim 21, which is directed to Figures 1A and 1C, has been further amended herewith to clarify the present invention. Specifically, claim 21 has been amended to recite that an exclusive wiring for a capacitance, in addition to a gate line, is provided for each pixel. Claim 21 is also believed to be allowable over the prior art of record for the reasons set forth herein.

For all of the above reasons, it is respectfully asserted that claims 1-3, 5-8, 21-22 and 24-27 are now in proper condition for allowance and reconsideration of the pending rejections is respectfully requested. If the Examiner believes that any further discussions would be beneficial in this case, it is requested that the undersigned be contacted.

Respectfully submitted,



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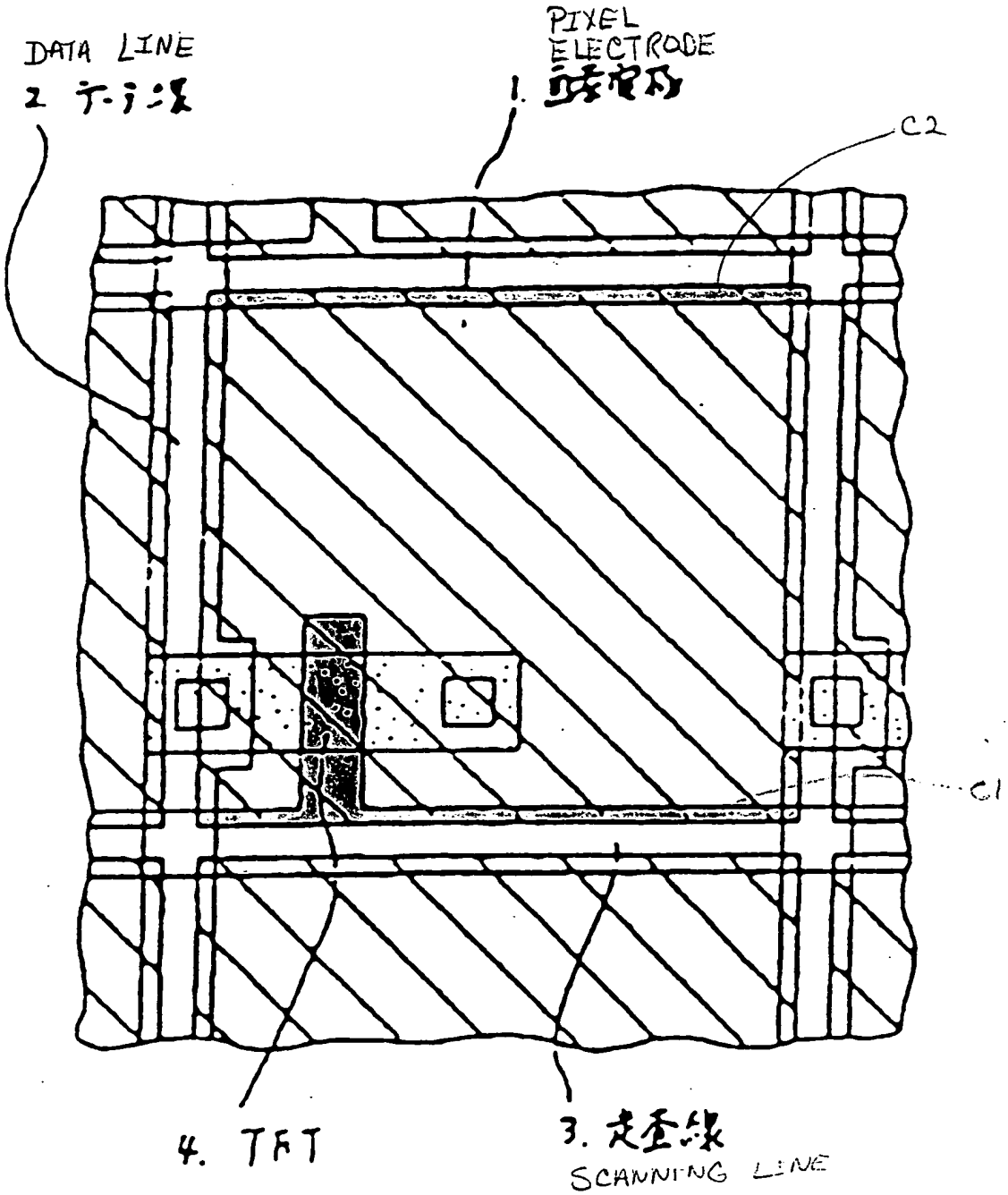
DATA LINE
2 データ線
PIXEL ELECTRODE
1. 画素電極
C2
C1
4. TFT
3. 走査線
SCANNING LINE

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